REMARKS

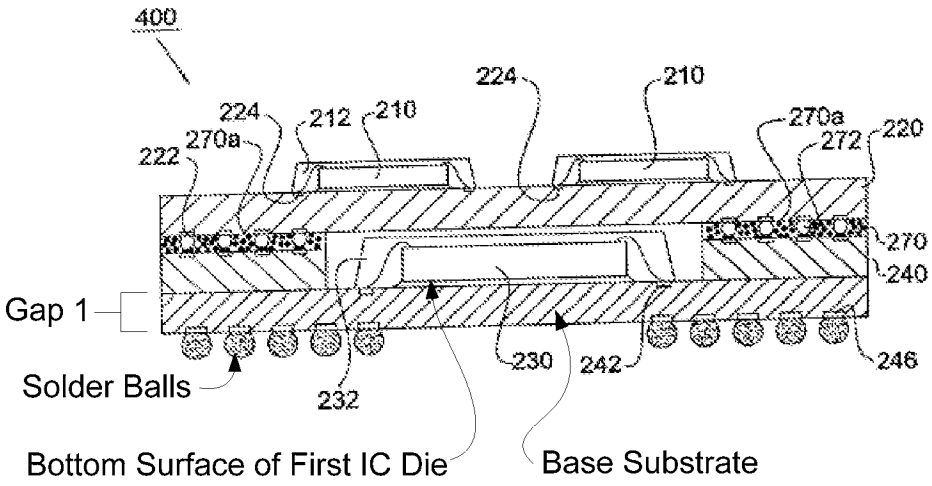
In the Claims:

Claims 15-17, 19-23, and 27-32 remain in this application. Claims 1-14 were previously canceled. Claims 18 and 24-26 have been withdrawn. No claims have been amended, canceled or added in this response.

Claim Rejections Under 35 U.S.C. 102(b):

Claims 15, 27-28, and 30 were rejected under 35 U.S.C. 102(b) as being anticipated by Chen (U.S. Pub. 2002/0158318) (hereinafter "Chen").

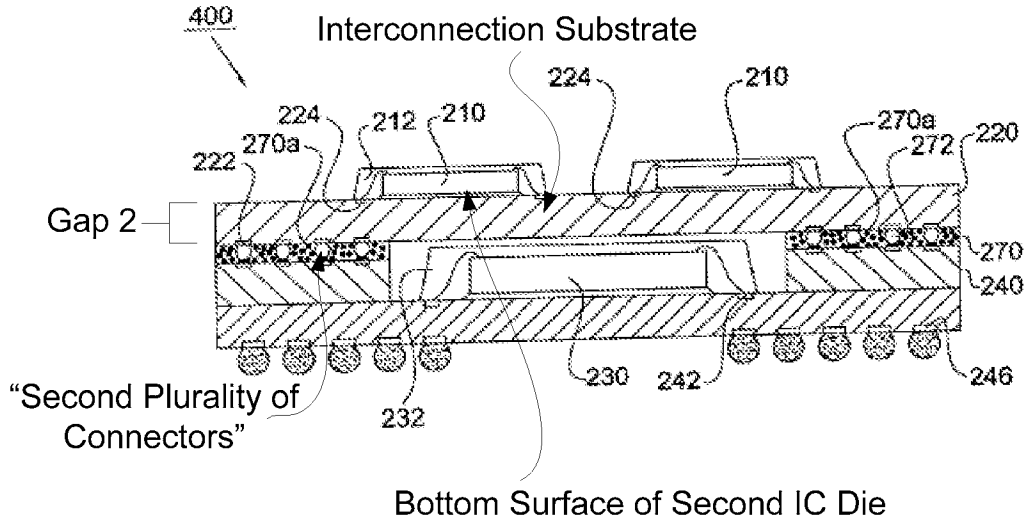
Chen fails to disclose that the first plurality of connectors extend from the top surface of the substrate to the bottom surface of the first integrated circuit die, as is recited in claim 15; the rejection is unsupported in the art and should be withdrawn. This can be seen by looking at Figure 4 of Chen, which is reproduced in annotated form below.



The Examiner has characterized lower chip 230 of Chen as the first integrated circuit die and solder balls attached to contacts 246 as the first plurality of connectors. However, the solder balls of Chen do not extend to the bottom surface of the first

integrated circuit die, as is recited in the claim. Rather, the bottom surface of the "first integrated circuit die" 230 of Chen is separated from the solder balls on connectors 246 by "Gap 1." The thickness of Gap 1 is approximately the thickness of base substrate 240. While in the Figure the reference number 240 points to the upper section of the base substrate, paragraph [0021] of Chen states that the base substrate 240 includes the contacts 246, which makes it clear that the lower portion beneath the lower chip 230 is also part of the base substrate 240. Thus, it is obvious that the solder balls on contacts 246 do not extend to the bottom surface of lower chip 230. Because they do not do so, but instead are separated by Gap 1, Chen fails to disclose each limitation of claim 15. The rejection should be withdrawn.

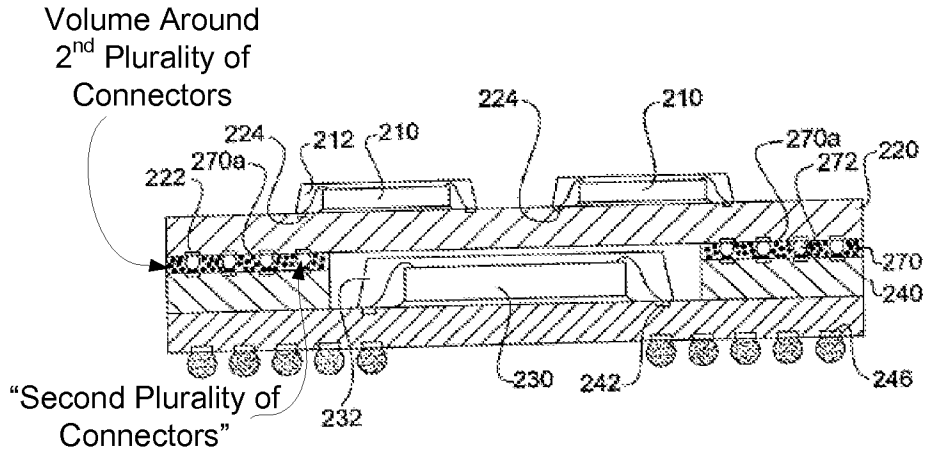
Further, Chen fails to disclose that the second plurality of connectors extend from the top surface of the first integrated circuit die to the bottom surface of the second integrated circuit die, as is recited in claim 15; the rejection is unsupported in the art and should be withdrawn. This can be seen by looking at Figure 4 of Chen, which is reproduced in a second annotated form below.



The Examiner has characterized upper chip 210 of Chen as the second integrated circuit die and metal bumps 272 as the second plurality of connectors. However, the metal bumps 272 of Chen fail to extend from the top surface of the first integrated circuit die to the bottom surface of the second integrated circuit die, as is recited in the claim. Rather, the bottom surface of the "second integrated circuit die" 210 of Chen is separated from the metal bumps 272 by "Gap 2." The thickness of Gap 2 is approximately the thickness of interconnection substrate 220. The Figure of Chen makes it obvious that the metal bumps 272 of Chen do not extend to the bottom surface of upper chip 210. Because they do not do so, but instead are separated by Gap 2, Chen fails to disclose each limitation of claim 15.

Claims 27 and 28 depend from claim 15. For the reasons provided above, the rejections of claims 27 and 28 are unsupported in the art and should be withdrawn.

Chen fails to disclose that the second volume between the first integrated circuit die and the second integrated circuit die and around the second plurality of connectors remains substantially free of the underfill material after sealing, as is recited in claim 30; the rejection is unsupported in the art and should be withdrawn. The Examiner characterized metal bumps 272 of Chen as the recited second plurality of connectors and adhesive film 270 shown in Figure 4 of Chen as the recited underfill material that seals the volume between the first and second integrated circuit dies (*see*, page 3 of Office Action dated Sept. 6, 2006). However, it is obvious in Figure 4 of Chen (reproduced in annotated form below) that the volume around the second plurality of connectors does not remain substantially free of the underfill material.



Rather than the volume around the second plurality of connectors remaining substantially free of underfill as recited in claim 30, the adhesive film 270 of Chen completely fills in the volume around the metal bumps 272. Thus, because Chen fails to disclose each limitation of claim 30 the rejection is unsupported in the art and should be withdrawn.

Claim Rejections Under 35 U.S.C. 103(a):

Claims 16-17, 19-21, 23, 29, and 31-32 were rejected under 35 U.S.C. 103(a) as being unpatentable over Chen in view of Beyne et al. (U.S. 6,566,745) (hereinafter "Beyne"), Jiang (U.S. 6,777,268) (hereinafter "Jiang"), and Lee (U.S. 6,613,606) (hereinafter "Lee").

Claims 16, 17, 19-21, 23, and 29 depend from claim 15. As discussed above, Chen fails to disclose each limitation of claim 15. Beyne, Jiang and Lee, together or separately, fail to rectify this deficiency.

Beyne fails to disclose or suggest the two integrated circuit dies and substrate arranged with the first die above the substrate and a second die above the first integrated circuit die, wherein the volume between the first and second integrated circuit dies are

substantially sealed from a surrounding environment, as is recited in amended claim 15. Beyne is concerned with a transparent cover attached to an imaging device, and does not disclose or suggest multiple integrated circuit dies connected as recited in amended claim 15.

Jiang fails to disclose or suggest the two integrated circuit dies and substrate arranged with the first die above the substrate and a second die above the first integrated circuit die, wherein the volume between the first and second integrated circuit dies are substantially sealed from a surrounding environment, as is recited in amended claim 15. Jiang is concerned with attaching a die 202 to a substrate 104 (Jiang, Figure 1), and not with stacked integrated circuit dies connected as recited in amended claim 15.

Lee fails to disclose or suggest dies stacked and connected as recited in amended claim 15. Instead of a first plurality of connectors forming an electrical connection between the substrate and the bottom surface of the first integrated circuit, in Lee a top surface of die (22) is connected to a bottom substrate (50) via a portion of substrate (10) that is above the die (22).

Thus, because none of the cited references disclose or suggest the arrangement and connection of integrated circuit dies recited in claim 15, the rejections of claims 16, 17, 19-21, 23, and 29 are unsupported in the art. Withdrawal of the rejection of claims 16, 17, 19-21, 23, and 29 is requested.

Further, claim 16 recites forming first and second "integrated circuit dies" and singulating them. Because the rejection fails to set forth any disclosure in the cited references of such singulated **integrated circuit** dies, no proper prima facie rejection has been made; the rejection should be withdrawn. The rejection states that Beyne discloses

forming singulated dies with connectors on each die (*see*, page 3 of Office Action dated Sept. 6, 2006). This is a mischaracterization of Beyne. Beyne discloses that the top "die" is simply a portion of a glass wafer or other transparent substrate 51 (Beyne, col. 7, lines 24-42), not an **integrated circuit** die. Thus, because Beyne does not disclose forming two integrated circuit dies as is recited in the claim, the rejection is unsupported in the art and should be withdrawn. Jiang and Lee fail to rectify this deficiency.

Additionally, Jiang fails to disclose or suggest filler particles having an average diameter greater than the second distance between the first die and second die, as is recited in claim 19. While the filler particles 266 of Jiang may get jammed between the semiconductor die active surface and the semiconductor substrate back surface (Jiang, col. 3, lines 30-35), Jiang sheds no light whatsoever on the average diameter of the filler particles, much less that the average diameter is greater than the second distance between the first die and second die. The rejection cites col. 3, lines 22-45 as supporting this rejection, but nowhere in that section does Jiang disclose anything at all about the **average** filler particle diameter. Applicants request that the Examiner either point out where Jiang discloses any information about the average filler particle diameter or withdraw the rejection.

Claims 31 and 32 depend from claim 30. As discussed above, Chen fails to disclose each limitation of claim 30. Beyne, Jiang and Lee, together or separately, fail to rectify this deficiency.

Further, no proper prima facie rejection of claim 32 has been made. the Examiner admits (*see*, page 5 of Office Action dated Sept. 6, 2006) that Chen does not disclose that sealing the device comprises applying a single layer of underfill material extending from

the substrate to the second integrated circuit die, the underfill being in contact with both the first and second integrated circuit dies, as is recited in claim 32. The Examiner states that Lee discloses that a layer of underfill extends from the substrate to the second integrated circuit die (*see*, page 6 of Office Action dated Sept. 6, 2006), but completely ignores the limitation recited in claim 32 that states, "the layer of underfill material being in contact with both the first and second integrated circuit dies." The underfill 53, of Lee, is not in fact in contact with both dies, as it is not in contact with die 22 (Lee, Figure 11). Thus, none of the cited references, alone or in combination, disclose each limitation recited in claim 32. The rejection is unsupported in the art and should be withdrawn.

Respectfully submitted,

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